Fig.1.

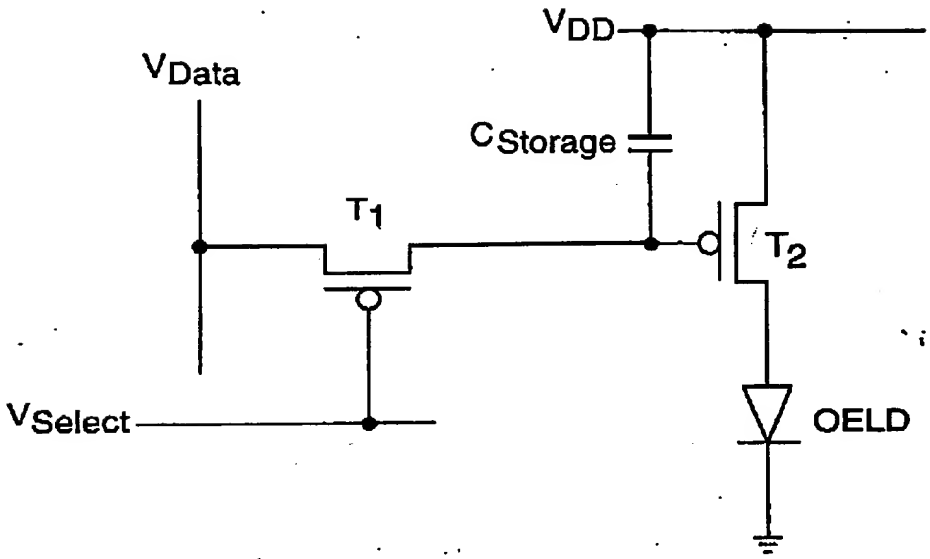
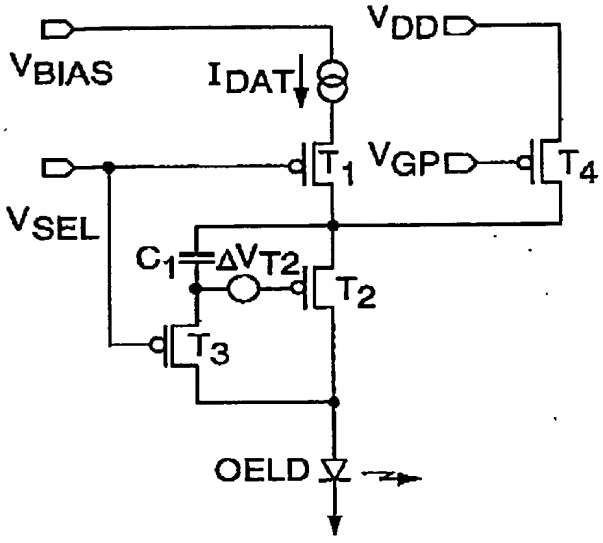

VDD
VData
CStorage
T1
T2
VSelect
OELD

Fig.2.


VDD
VBIAS
IDAT
T1
VGP
T4
VSEL
C1
ΔVT2
T2
T3
OELD

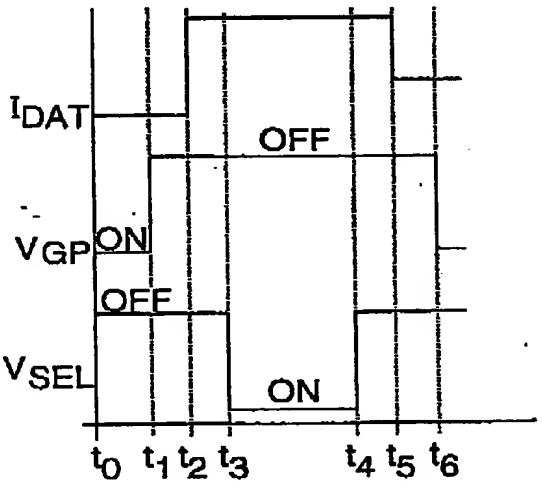

IDAT
OFF
VGP
ON
OFF
VSEL
ON
t0 t1 t2 t3 t4 t5 t6

Fig.3.

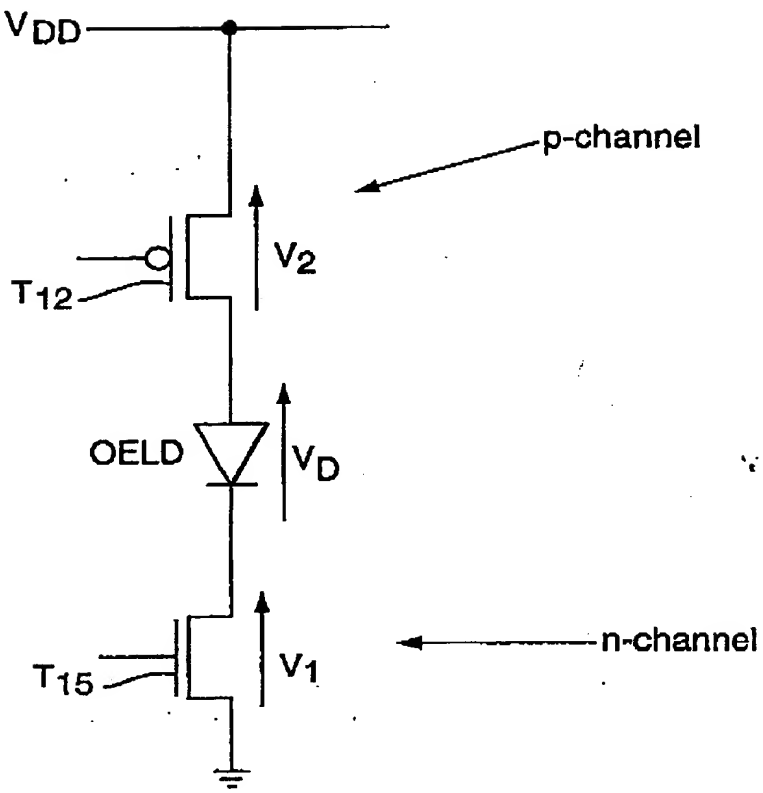

VDD
p-channel
V2
T12
OELD
VD
T15
V1
n-channel

Fig.4.

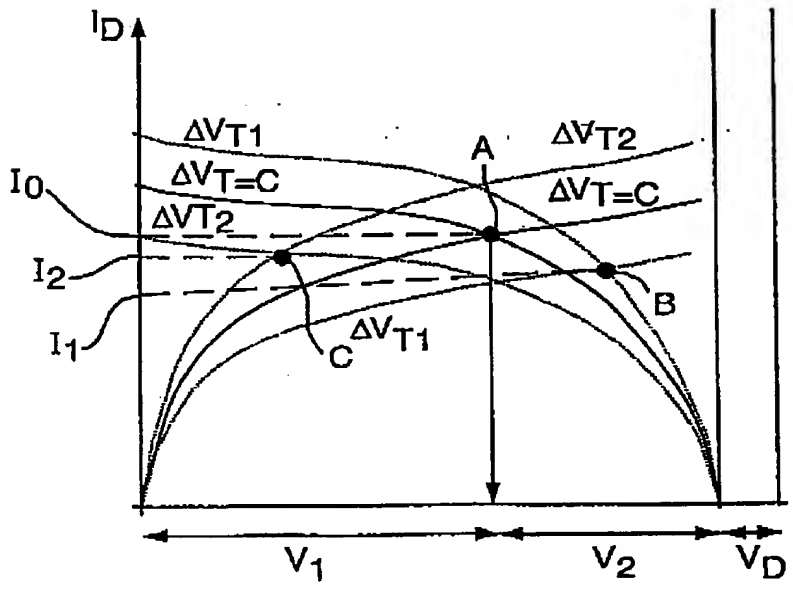

ID
ΔVT1
A
ΔVT2
I0
ΔVT=C
ΔVT=C
ΔVT2
I2
B
I1
C
ΔVT1
V1
V2
VD

Fig.5.

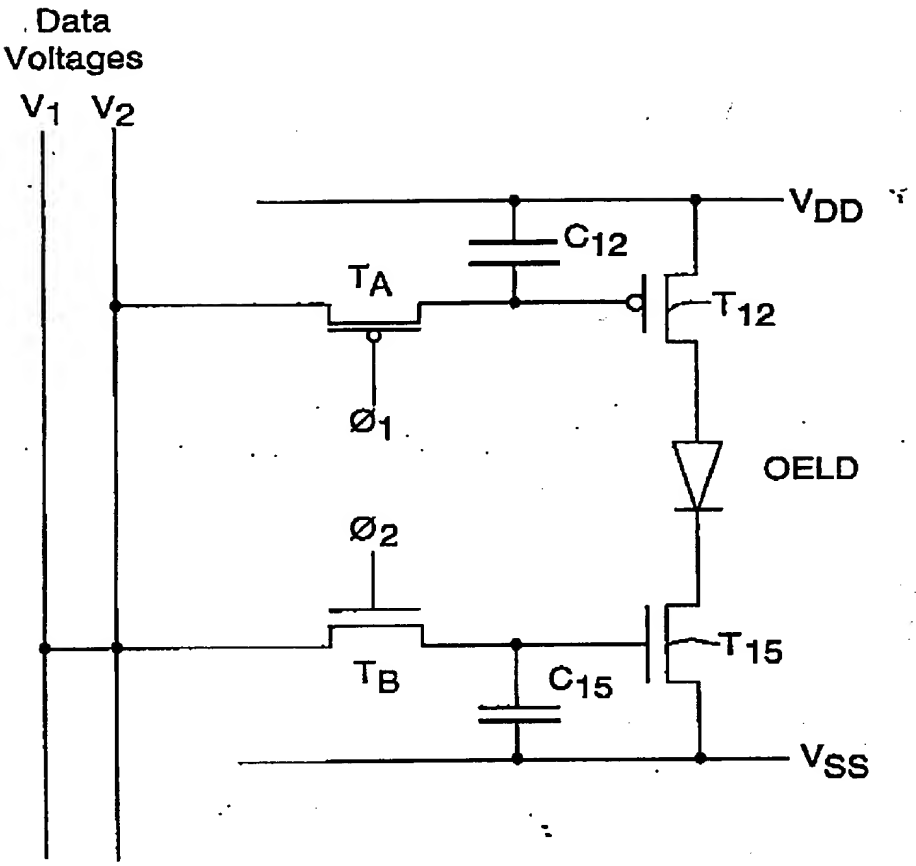
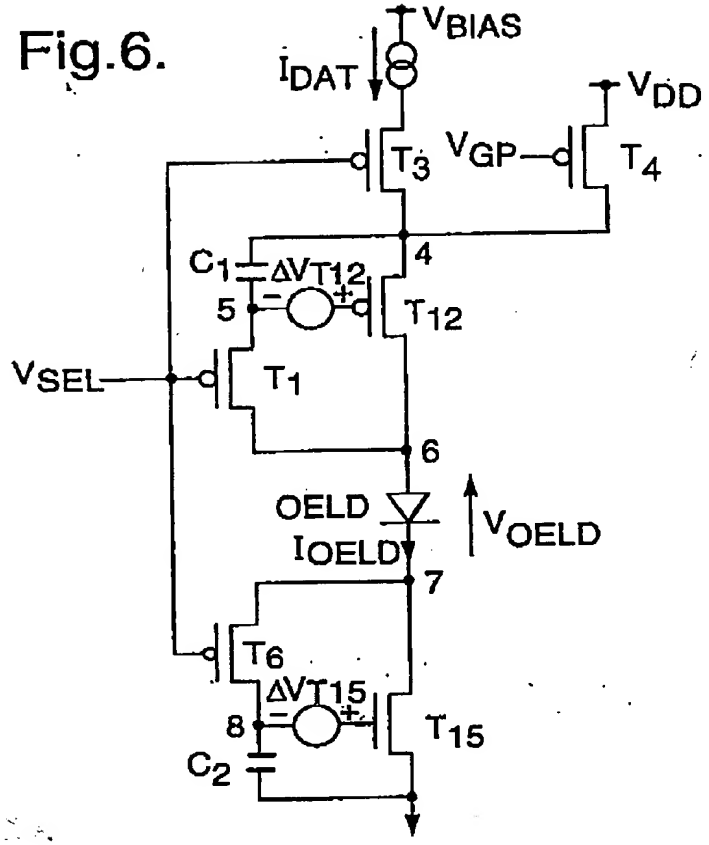


Fig.6.


VBIAS
IDAT
VDD
T3
VGP
T4
C1
ΔVT12
4
5
T12
VSEL
T1
6
OELD
VOELD
IOELD
7
T6
ΔVT15
8
T15
C2

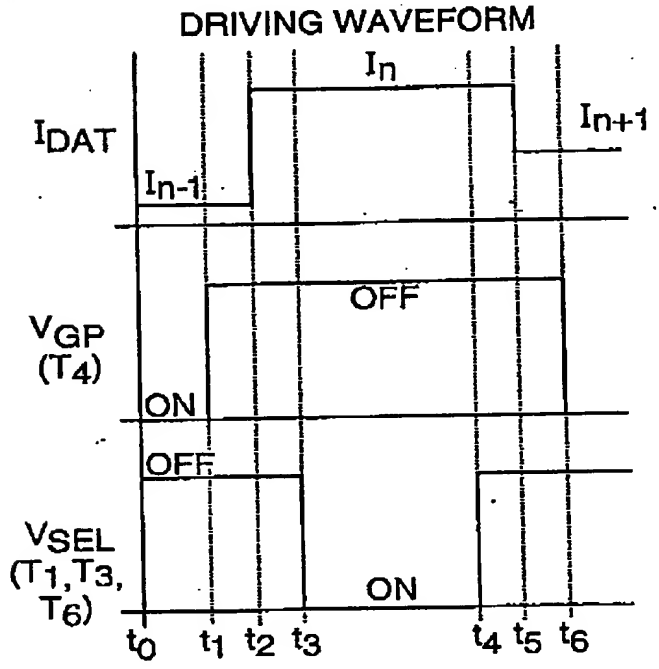
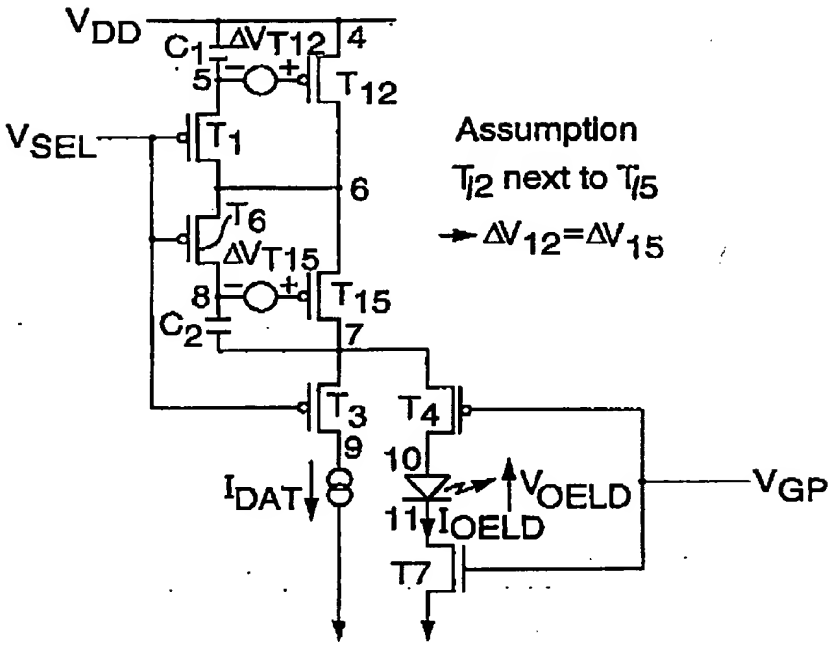

DRIVING WAVEFORM
In
IDAT
In+1
In-1
OFF
VGP
(T4)
ON
OFF
VSEL
(T1,T3,
T6)
ON
t0
t1
t2
t3
t4
t5
t6

Fig.7.


VDD
C1
ΔVT12
4
5
T12
VSEL
T1
Assumption
Tj2 next to Tj5
→ΔV12=ΔV15
6
T6
ΔVT15
8
T15
C2
7
T3
T4
9
10
IDAT
VOELD
VGP
11
IOELD
T7

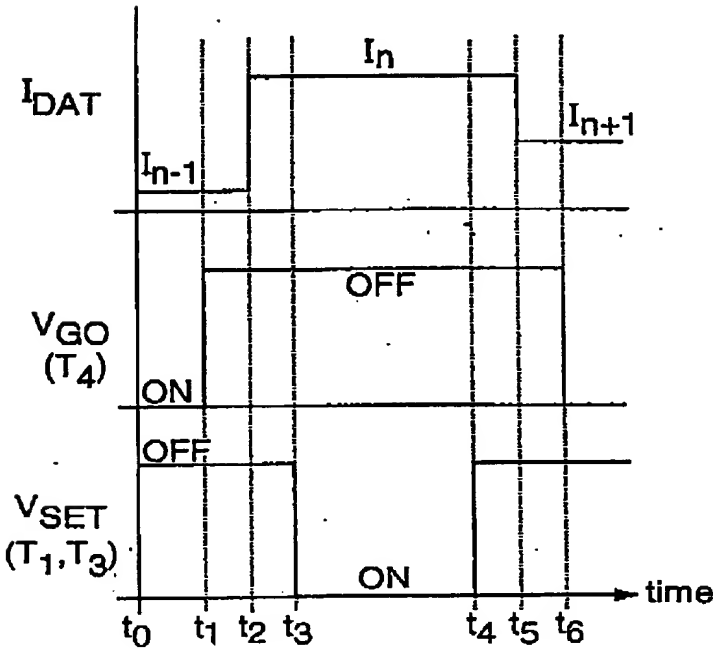

IDAT
In
In+1
In-1
OFF
VGO
(T4)
ON
OFF
VSET
(T1,T3)
ON
time
t0
t1
t2
t3
t4
t5
t6

Fig.8. SPICE Simulation Result ($V_{DD}$ =12.5V, $I_{DAT}$=1μA)

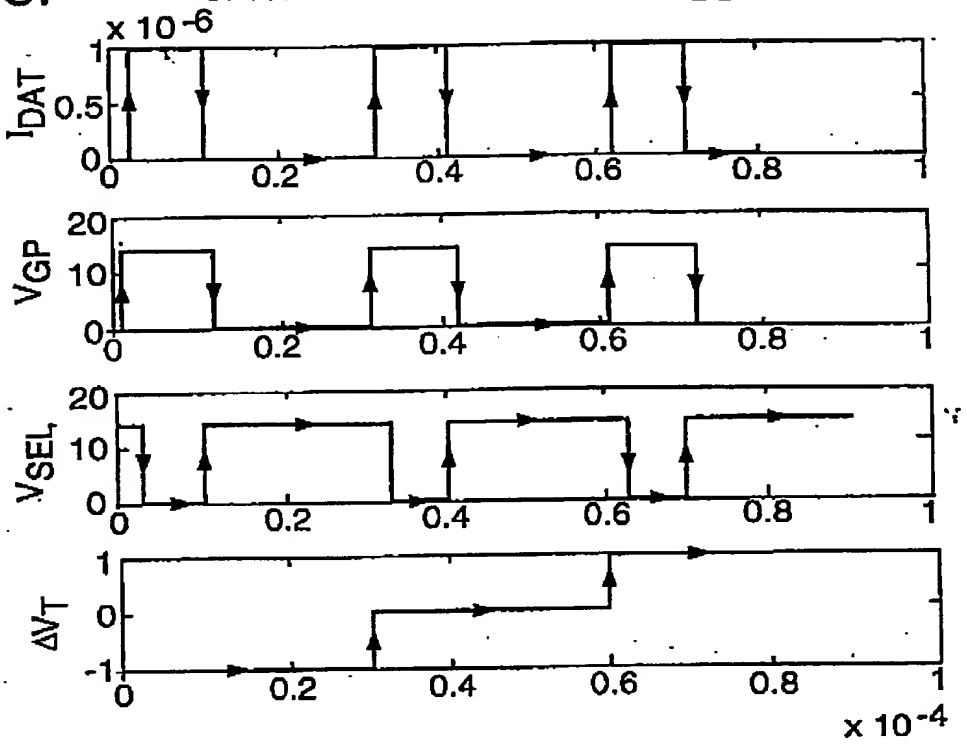



Fig.9.

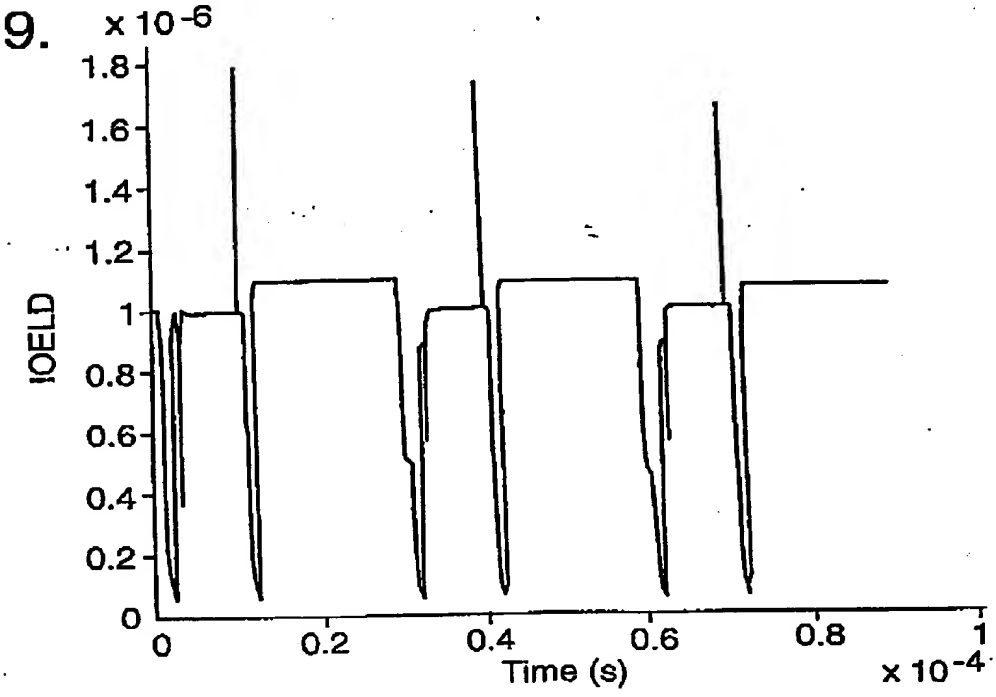


Fig.10.

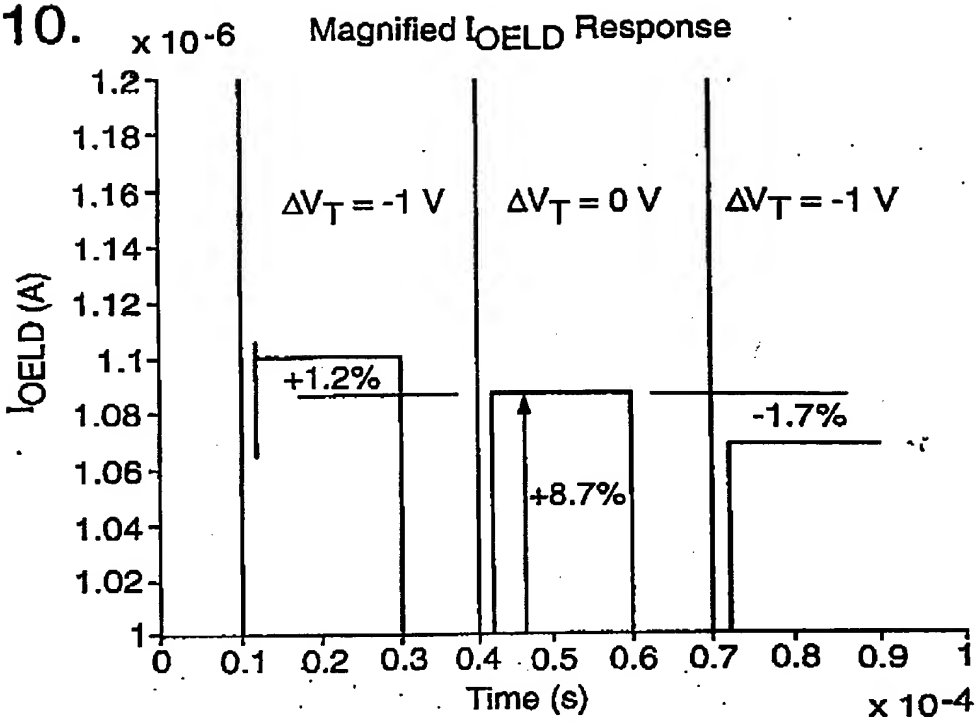

x 10-6
Magnified IOELD Response
1.2
1.18
1.16
1.14
1.12
1.1
1.08
1.06
1.04
1.02
1
IOELD (A)
ΔVT = -1 V
ΔVT = 0 V
ΔVT = -1 V
+1.2%
+8.7%
-1.7%
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Time (s)
x 10-4

Fig.11.

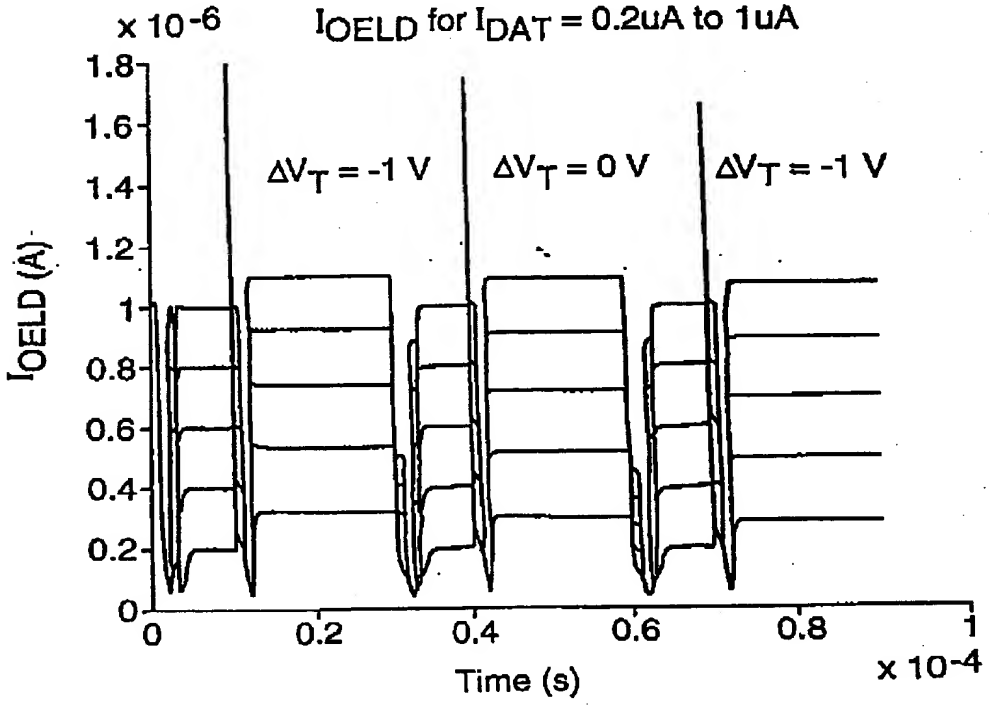

x 10-6
IOELD for IDAT = 0.2uA to 1uA
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
IOELD (A)
ΔVT = -1 V
ΔVT = 0 V
ΔVT = -1 V
0
0.2
0.4
0.6
0.8
1
Time (s)
x 10-4

Figure 12

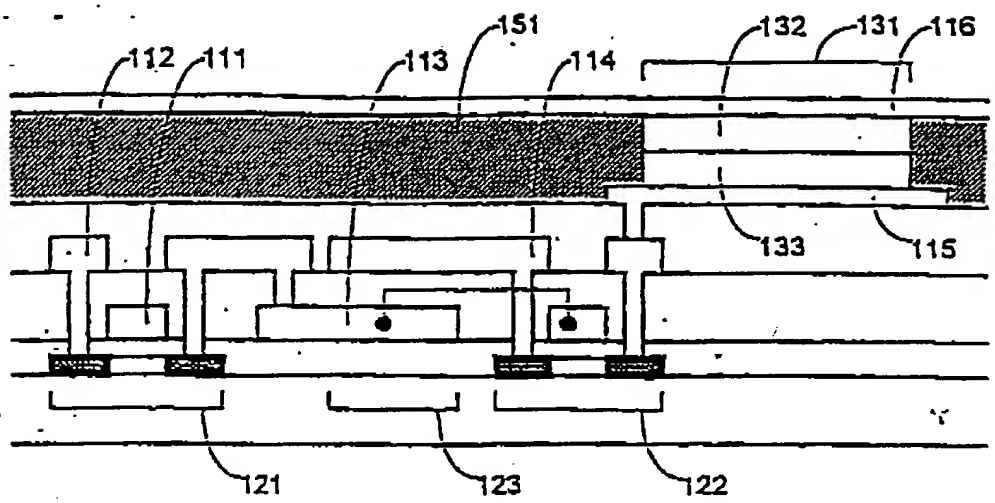
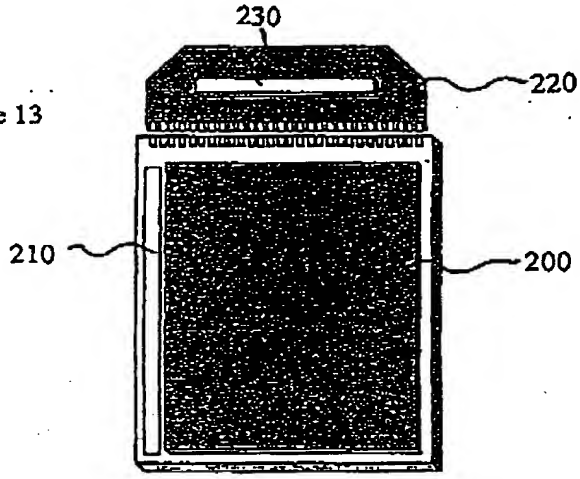



Figure 13



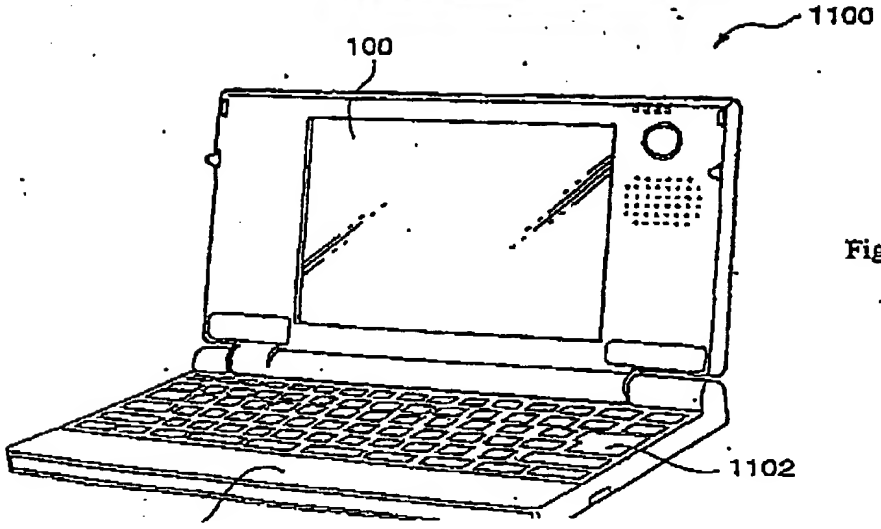




Figure 14

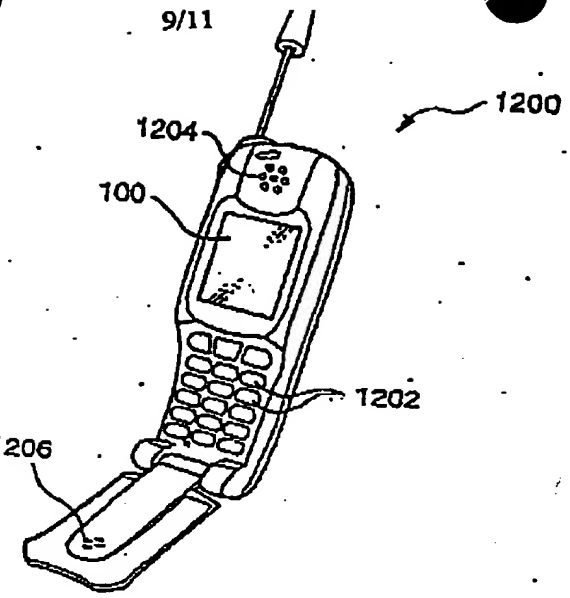



Figure 15

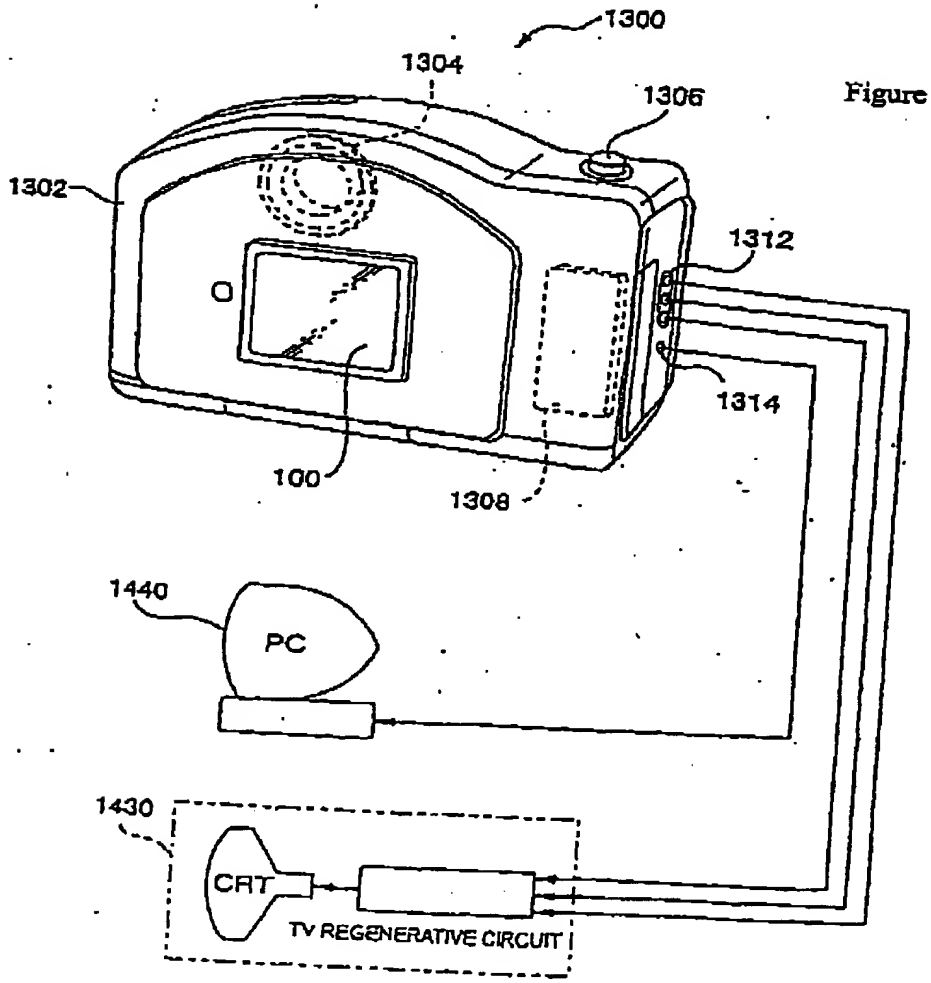



Figure 16

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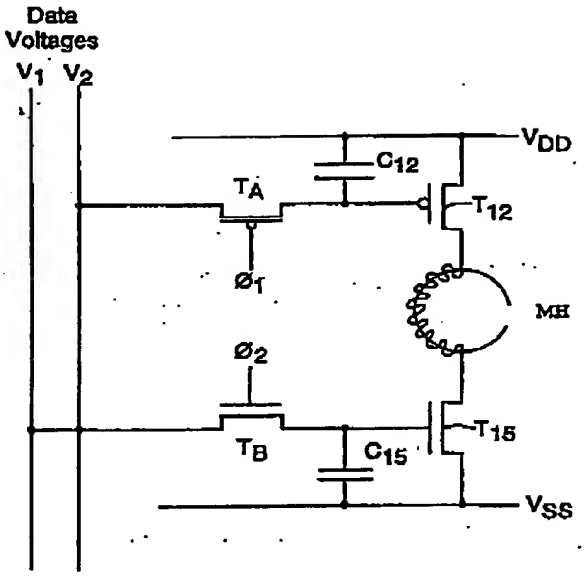


Figure 17

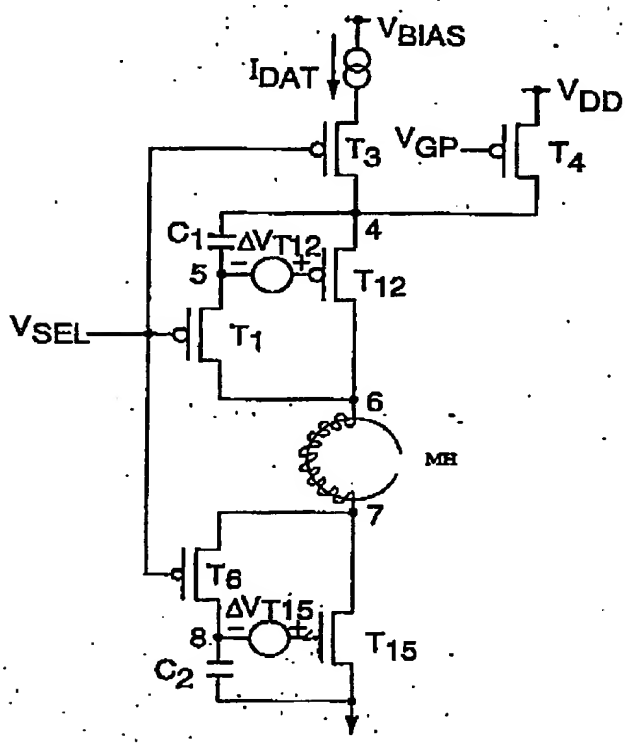


Figure 18

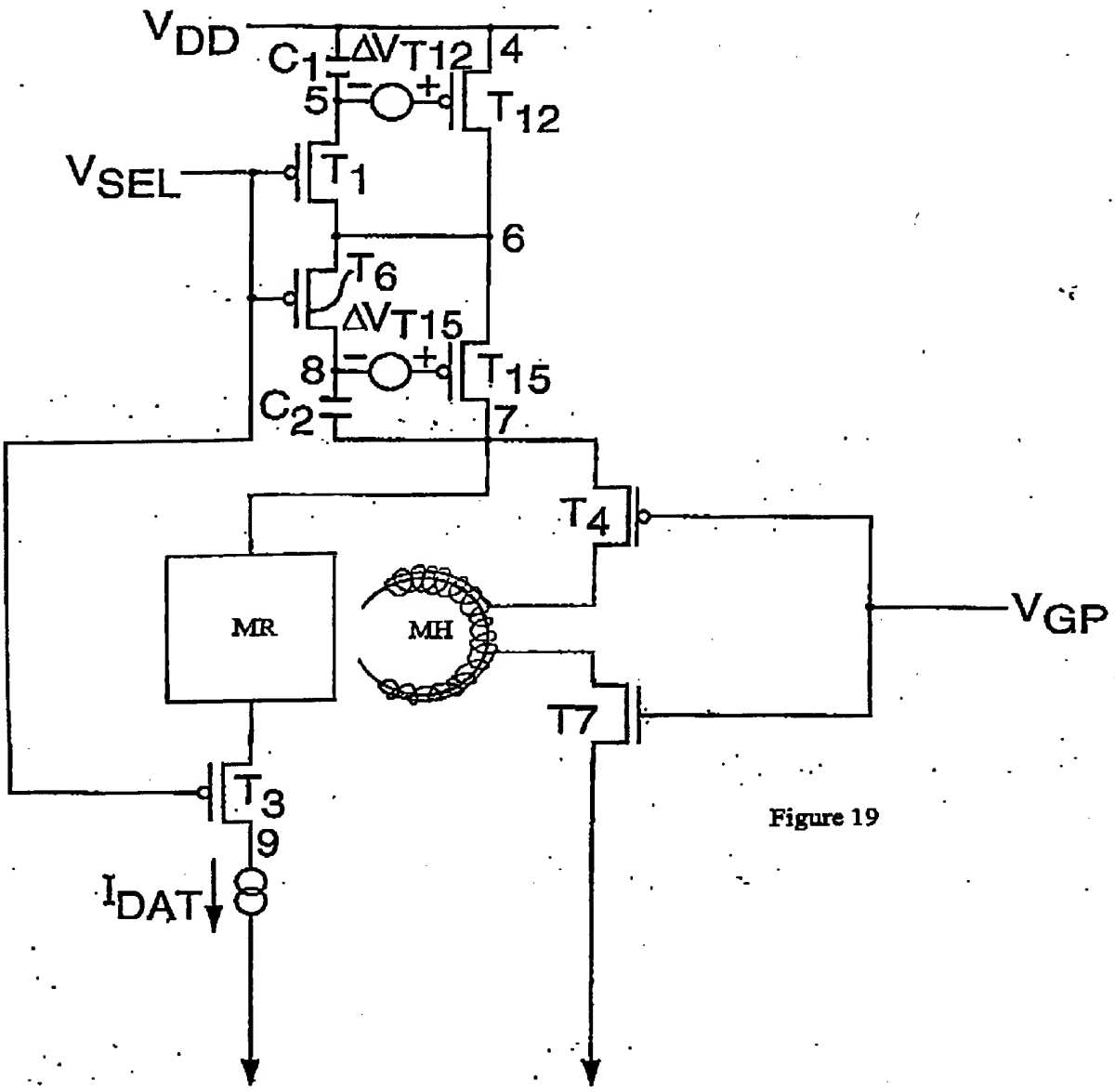
VDD
C1
ΔVT12
4
5
T12
VSEL
T1
6
T6
ΔVT15
8
T15
C2
7
T4
MR
MH
VGP
T7
T3
9
IDAT

Figure 19